

# Dataflow-based Adaptation Framework with Coarse-Grained Reconfigurable Accelerators

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## ABSTRACT

Today, the demand of adaptive systems is constantly growing, especially in hard-constrained contexts such as Cyber-Physical Systems. However, the efficient management of such platforms requires dealing with several issues such as the real-time execution, energy saving and dynamic context changes. Such strict requirements imply a high flexibility of the application and of the architecture on which it is executed. Runtime managers offer the possibility to dynamically schedule and map an application on the available software processing units. However, hardware acceleration may also be necessary for computationally-intensive workloads that depend on the running functionality, additionally complicating runtime management. Coarse-Grained Reconfigurable (CGR) accelerators have the ability to switch among different domain-specific functionalities with a small overhead. To support energy and time adaptivity in heterogeneous systems, and to exploit multi-core architectures and CGR accelerators, this work proposes the combination of the SPIDER software runtime manager and the dataflow-to-hardware MDC design suite for CGR accelerators.

## MOTIVATION

### SPIDER

Scheduling & Mapping @ Runtime  
SW Reconfigurability  
Dataflow-based  
Multi-core Architectures  
Open Source

**HW/SW Adaptivity**

**Dataflow-based**

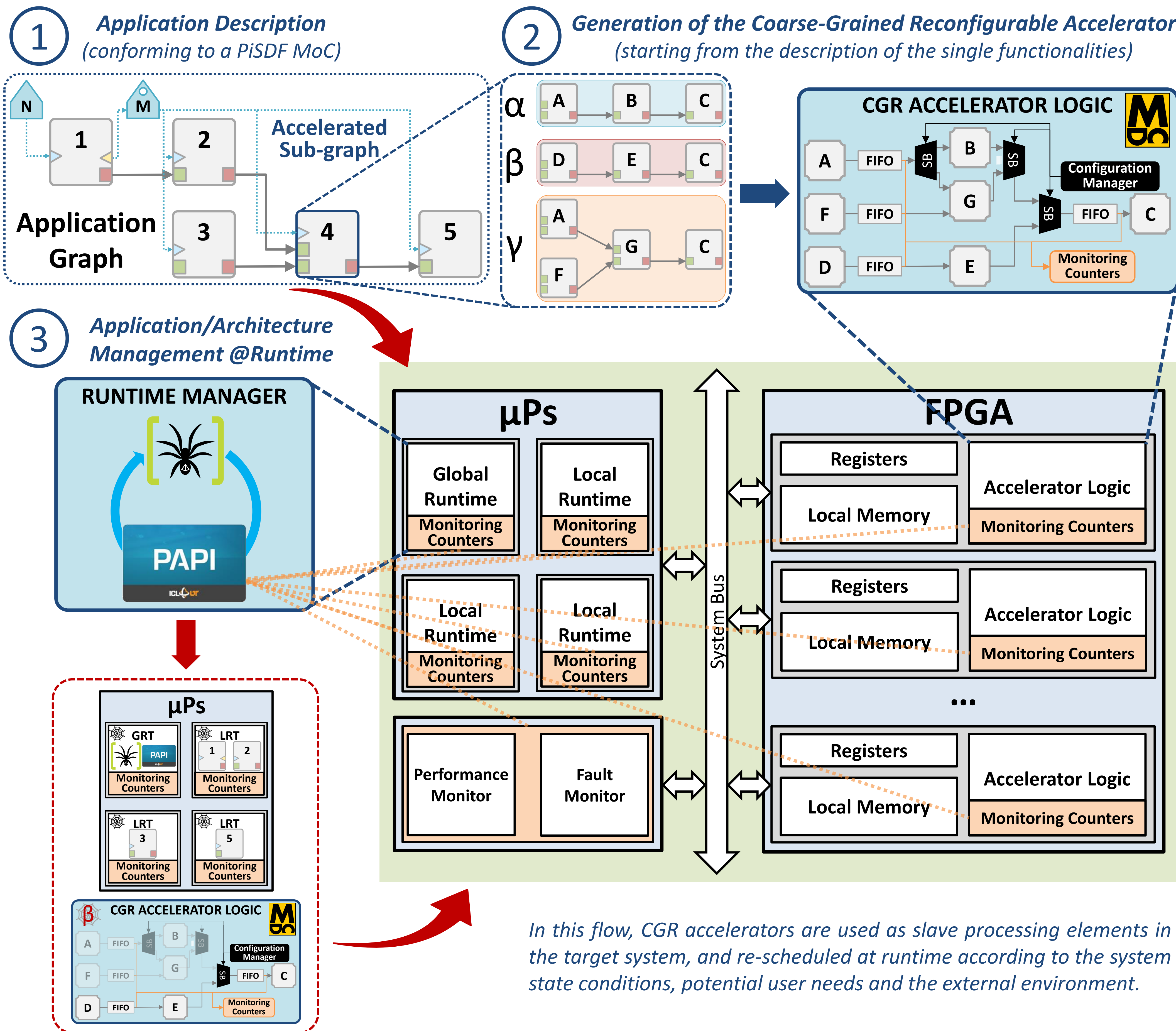
**Multi-core + CGR Accelerators**

**Open Source**

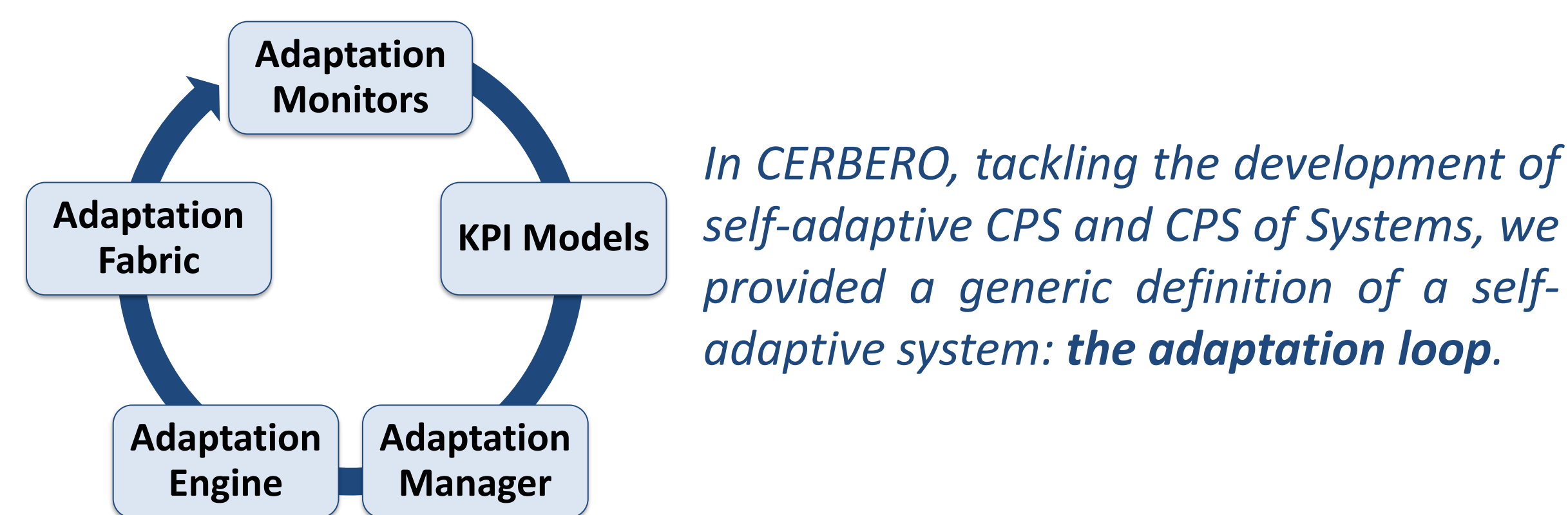
### MDC

Datapath Merging  
HW Reconfigurability  
Dataflow-based  
CGR Accelerators Generation  
Power management  
Open Source

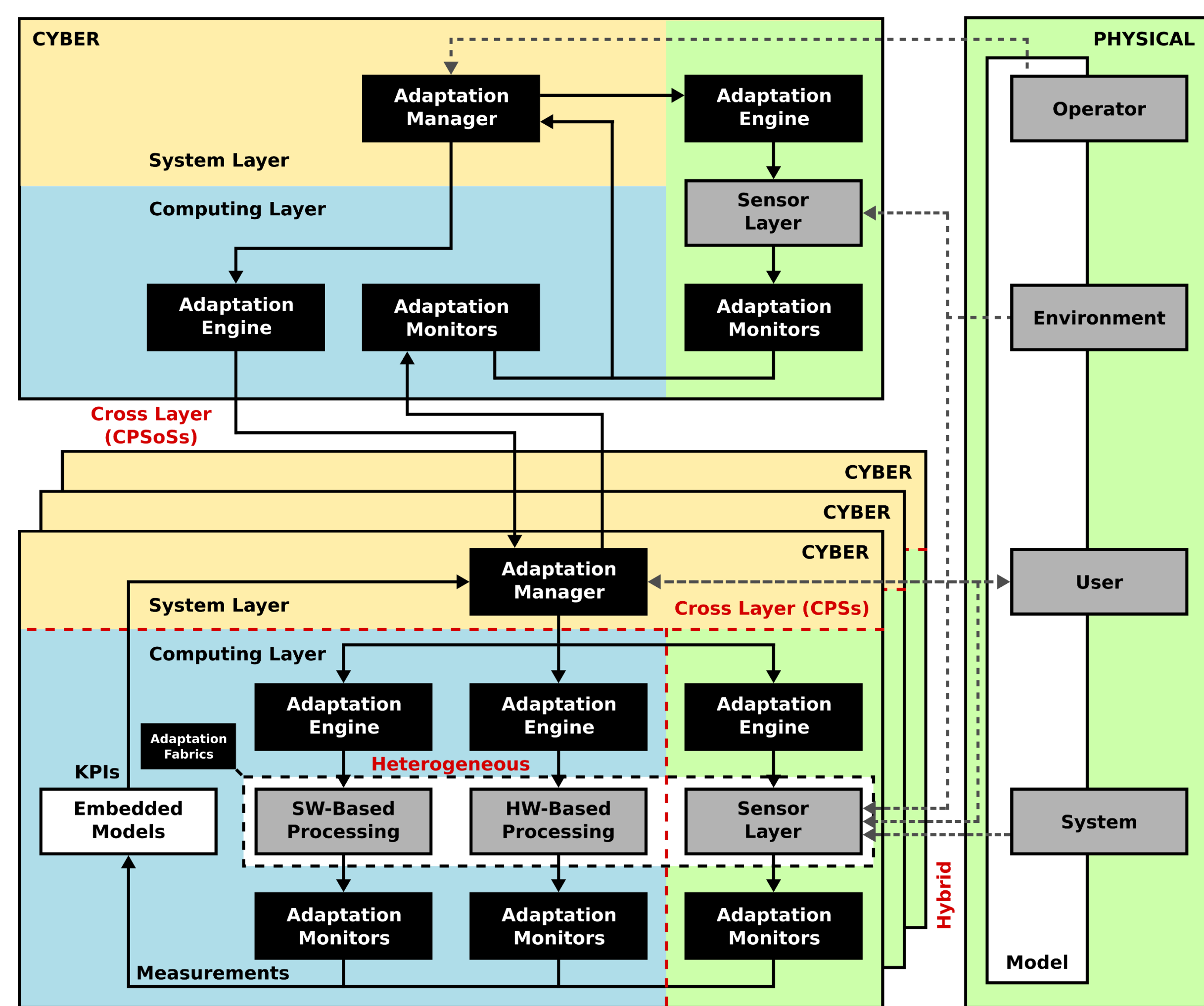
## CGR ADAPTATION FLOW



## Self-Adaptivity in CERBERO H2020



CERBERO adaptivity support is based on a *multi-layer heterogeneous (HW-SW) autonomous engine*



## OVERVIEW

### Challenges

**HW/SW Adaptivity** for systems requiring low energy and time overheads.

**Performance Predictability** related to the different configurations of the system.

**HW/SW Fault Robustness** in architectures composed of heterogeneous processing elements.

### Strategies

**CGR Acceleration:** to switch among different functionalities of computationally-intensive workloads with low time overheads.

**Modeling:** a strategy based on models of architecture and chosen applications will be used to achieve performance predictability.

**HW/SW Monitoring:** to provide feedback to SPIDER about the current execution of the hardware and software tasks.

### Research Plan

**Step 1:** Integrate MDC and SPIDER by combining software and hardware adaptation according to variable application parameters.

**Step 2:** Verify this approach with respect to relevant CERBERO key performance indicators (such as energy, latency, and throughput).

**Step 3:** Derive a proof of concept of the proposed approach in the context of CERBERO project use case scenarios.