IEEE Denmark EMC Society

DESIGN OF AN EMC FILTER FOR AN AUTOMOTIVE ON BOARD CHARGER

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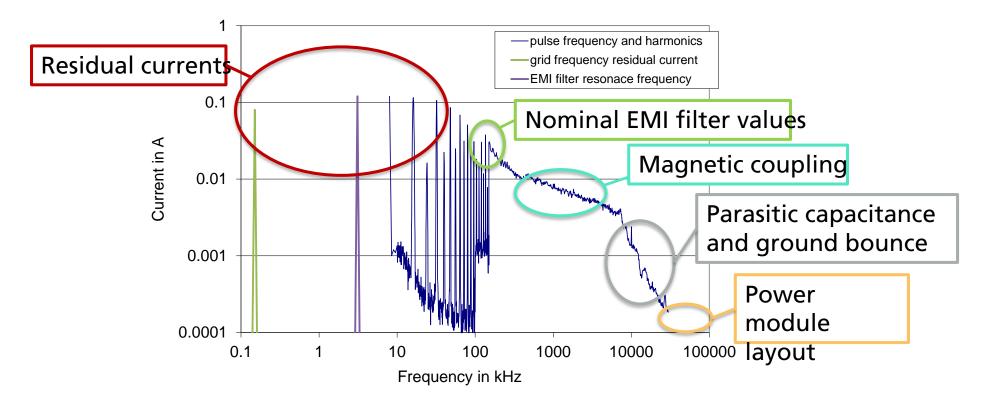


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Which EMI effects can be simulated to accelerate the design process?

Power electronics always generate interference, because they transform energy by switching. These effects are mostly evaluated in frequency domain and ways of prediction shall be demonstrated.

Different effects dominate depending on the frequency and simulation methods have to be adapted accordingly



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Which EMI effects can be simulated to accelerate the design process?

	Simulation complexity*	Modeling effort*	Unknown parameters	Expert knowledge*
Residual currents	3	3	Grid properties	4
Nominal filter values	3	4	many	5
Magnetic coupling	8	8	many	8
Parasitic capacitance	3	3	medium	4
Ground bounce	8	8	very many	10
Radiated emissions/ power module layout	8	10	very many	10

Today's talk

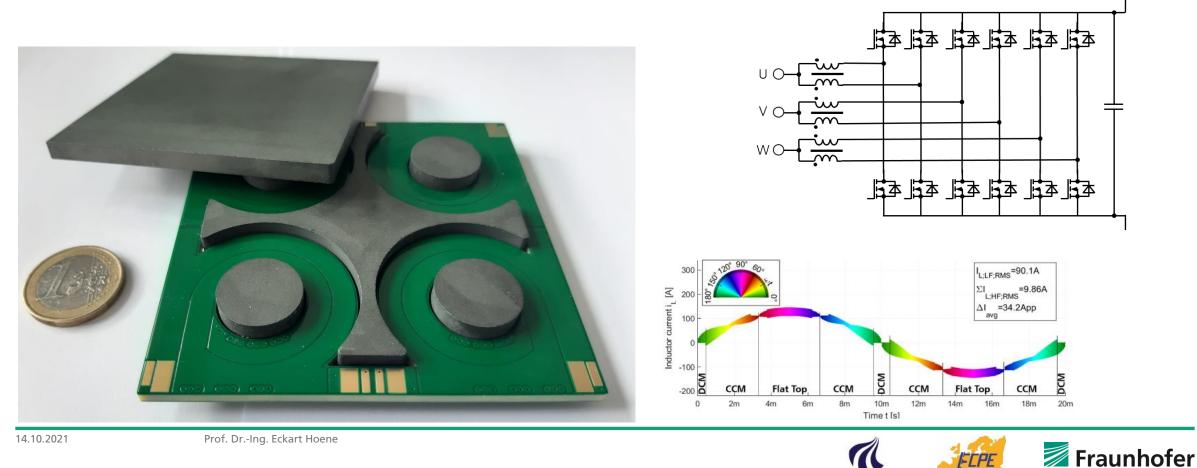
* On a scale of 0 (low) to 10 (high)



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Practical example: 3-phase PFC for a 22kW OBC

- Two interleaved half bridges for each phase, 1200V SiC semiconductors, PCB based coupled inductor, 140kHz switching frequency
- Optimization goal: a EMI filter to comply with the EMI standards and to fulfill the 2.5mA residual current limit (this limits the y-capacitors to a total value of about 47nF)

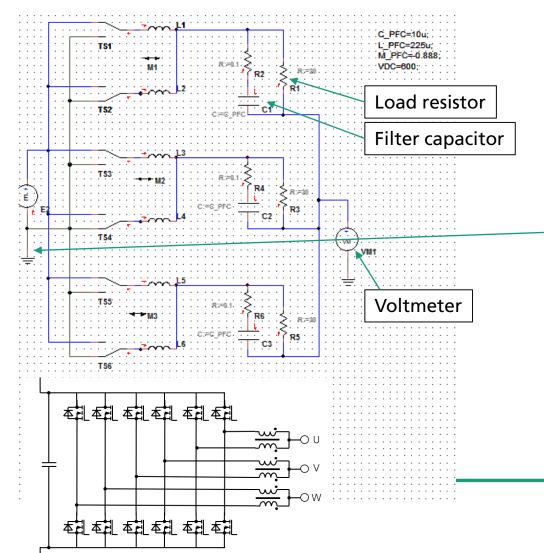


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1st step: Setting up a functional simulation in time domain

- Select a circuit simulator with good simulation stability, e.g. Portunus or Simplorer (not SPICE)
- Model semiconductors as ideal switches, add inductors, filter capacitors and a load



One very important influence is the ground connection

- In this example a hard ground connection for the DC link is assumed. Then the filter has to take the full common mode voltage and gets significantly bigger. In many OBCs the DC/DC converter decouples the DC link from ground. Then this connection has to be replaced by the parasitic coupling capacitance of the transformer
- Parasitic capacitance between transistors and heat sink will be added later





1st step: Setting up a functional simulation in time domain

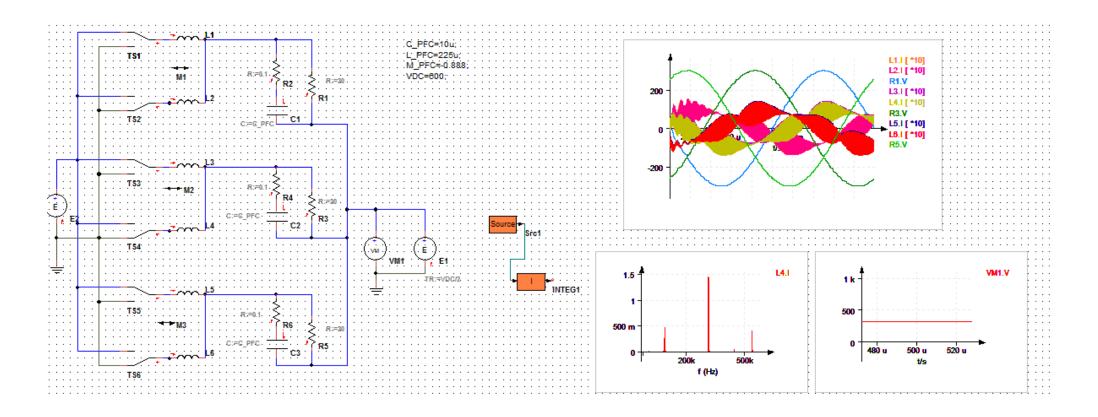
Pulse pattern generation Voltages and currents f(t) Triang. U Dr f(t) sine SINE1 TS1 L1.I [*10] 12.1 [*10] f(t) Triang. U Dr180 R1.V (t) sine SINE120 L3.1 [*10] 200 L4.I [*10] Load resistor f(t) sine SINE24 R3.V L5.I [*10] Filter capacitor 200 R3 **Current harmonics** Common mode voltage 141 VM1.V 1.5 -INTEG1 Voltmeter 500 m 200 200k 500 490 u 500 u f (Hz) Inductor flux The common mode diagram depicts the CM voltage generated by INTEG1.OUT this circuit, which has to be filtered 50 u Clamping the star point of the 3 phases would be one solution to handle these voltages (next slides) -100 u 14.

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Add a pulse pattern generation and let it run

1st step: Setting up a functional simulation in time domain

• Clamped star point: the current stress in the main inductors gets higher, the higher the DC voltage the more significant

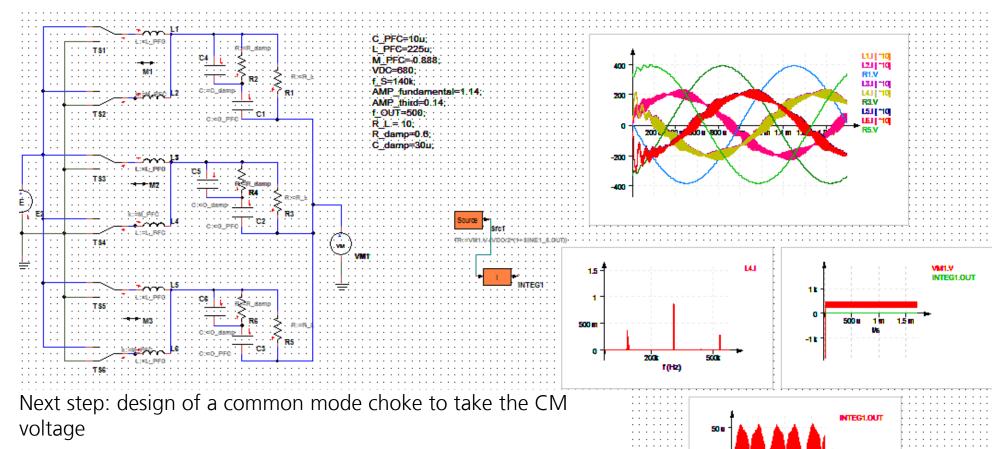




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1st step: Setting up a functional simulation in time domain

• Parameter adjustment: 3rd harmonic implementation and higher DC link voltage-> significant inductor current reduction



 Max. flux taken from simulation: 160µVs, thermally effective about 120µVs



Next step: design the first common mode inductor

- Max. flux taken from simulation: 160μVs, thermally effective about 120μVs (at 280 kHz)
- This is a high excitation, therefor a loss optimized ferrite has to be used, e.g. N87 from TDK

Uncoate Dimensior	d / epoxy coa	ting	R 58.3 × 32.0 × 18.0 (mm) R 2.295 × 1.260 × 0.709 (inch)			
d _a (mm)	d _i (mm)	Height (mm)	d _a (inch)	d _i (inch)	Height (inch)	
	32.0 ±0.7	18.0 ±0.5	2.295 ±0.039	1.260 ±0.028	0.709 ±0.020	uncoated ¹
58.3 ±1.0						

	A _L value	μ _i	~	Magneti	c charact	eristics		Approx.
rial		(approx.)		ΣΙ/Α	l _e	A _e	Ve	weight
	nH			mm-1	mm	mm ²	mm ³	g
K10	1500 ±25%	700	B64290A0043X010	0.58	134.0	230.0	30710	160
N87	4800 ±25%	2200	B64290L0043X087					

First try:

- ring core R58
- With 5 turns and a linked flux of 120µVs a flux density of 100mT is reached ☺

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- Core losses calculation: Ve * Pv = 30170mm³ * 390kW/m³ = 12W ☺
- With 7 turns losses reduce, core losses depend by the power of 2.2 from the amplitude: 5^2.2/7^2.2=0.48
- 5.7W core losses, with 2.5mm dia wire
 2.6W copper losses add: better solution

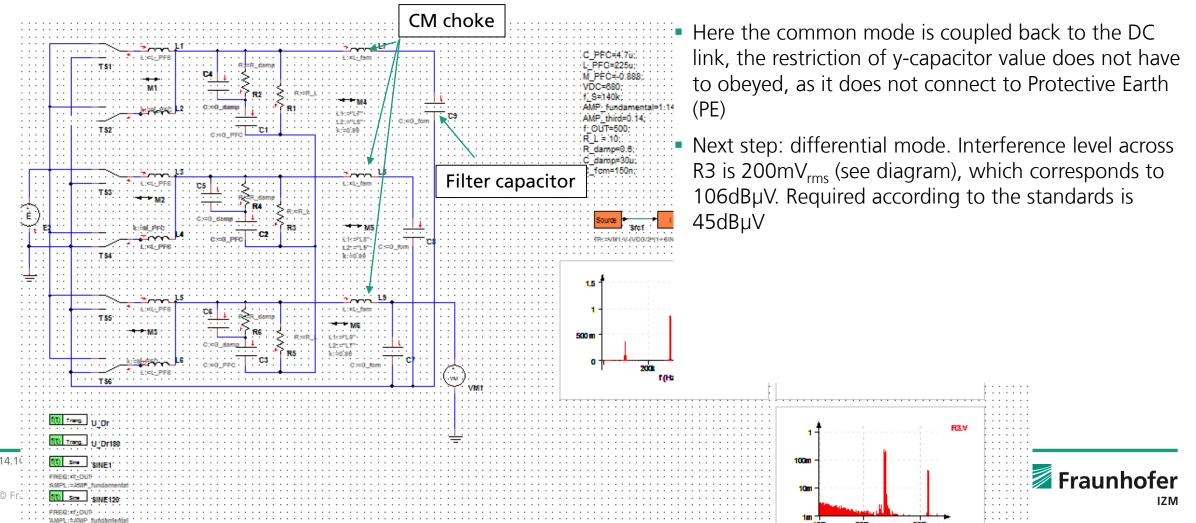
SIFERRIT materials	
N87	

Material properties

Preferred application	Power transformers N87		
Material			
Base material		MnZn	
	Symbol	Unit	
Initial permeability (T = 25 °C)	μ		2200 ±25%
Flux density (H = 1200 A/m, f = 10 kHz)	B _S (25 °C) B _S (100 °C)	mT mT	490 390
Coercive field strength (f = 10 kHz)	H _c (25 °C) H _c (100 °C)	A/m A/m	21 13
Optimum frequency range	f _{min} f _{max}	kHz kHz	25 500
Hysteresis material constant	η _Β	10- ⁶ /mT	<1.0
Curie temperature	T _C	°C	>210
Mean value of α _F at 25 … 55 °C		10- ⁶ /K	4
Density (typical values)		kg/m ³	4850
Relative core losses (typical values)	P _V		
25 kHz, 200 mT, 100 °C		kW/m ³	57
100 kHz, 200 mT, 100 °C		kW/m ³	375
300 kHz, 100 mT, 100 °C		kW/m ³	390
500 kHz, 50 mT, 100 °C		kW/m ³	215

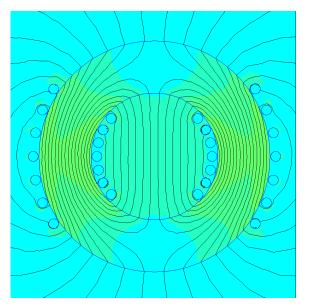
Select a capacitor to form a filter

- The nominal inductance of the common mode choke is $AI*N^2 = 4800nH*49 = 235\mu H$
- A decent filter stage should achieve 40dB: choke impedance at 280 kHz is 413Ω, so the capacitor should have 100 times less impedance (40dB), this is 4.1Ω or 140nF



Differential mode filter

The stray inductance of the choke is used for differential mode filtering

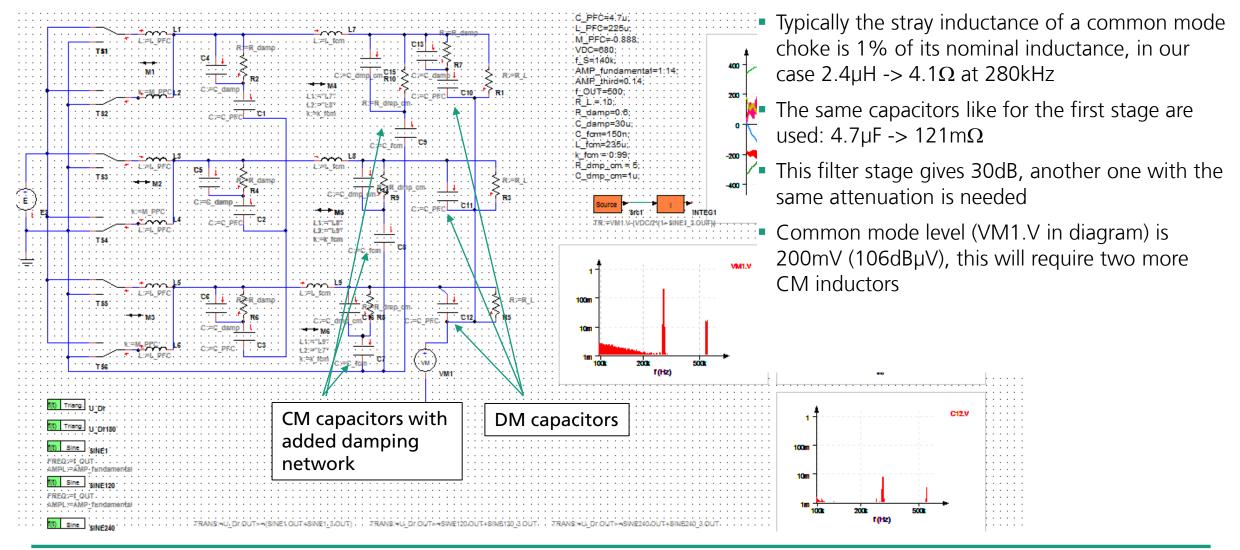


- Typically the stray inductance of a common mode choke is 1% of its nominal inductance, in our case 2.4μ H -> 4.1Ω at 280kHz
- The same capacitors like for the first stage are used: 4.7μF -> 121mΩ
- This filter stage gives 30dB, another one with the same attenuation is needed

Stray field lines of a 2 phase common mode choke



Filter topology up to now

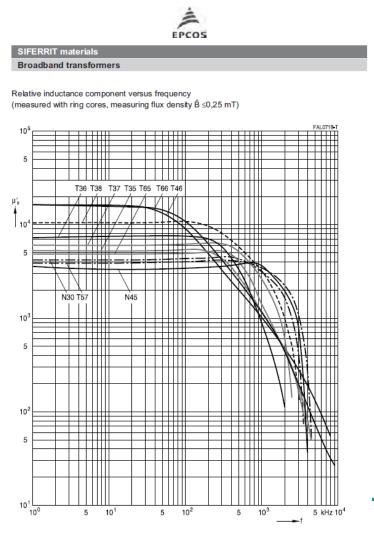


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Second common mode inductor

• This common mode choke is not loss limited any more, the focus is on high impedance



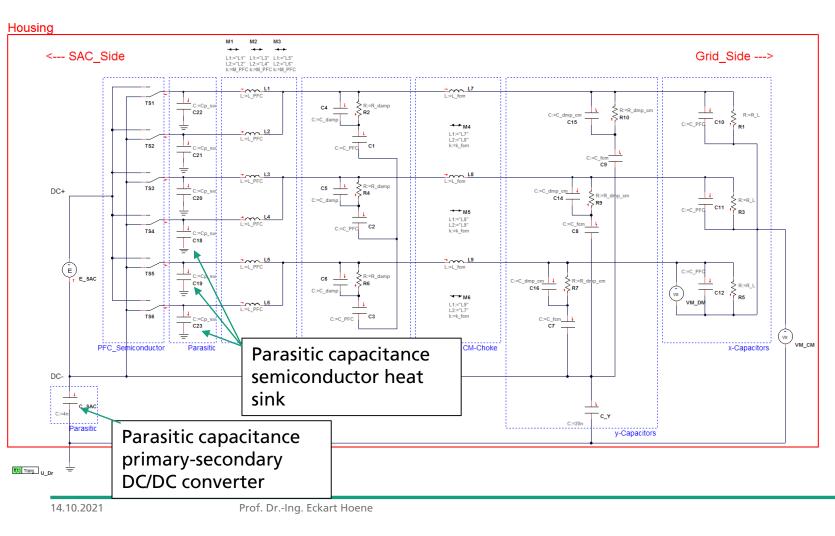
Selection:

- ring core R58, material T38 for highest impedance at 280kHz
- 7 turns results in 833 μ H, 1500 Ω at 280kHz
- 20nF y-caps are 28.4 Ω , this results in a damping of 34dB (->72dB μ V)
- In this topology a 3rd CM inductor is needed to fulfill the required 45dBµV. The same type is used, it damps together with the grid impedance represented by the LISN another 39dB
- For DM same procedure has to be carried out as shown before
- Now parasitic capacitances to ground have to added



Parasitic ground capacitance

• A colleague redrew my schematic...



Result

- The designed filter is sufficient even with added parasitics
- In this filter topology the first CM choke takes the full CM voltage. Modifications with no connection of filters to the DC link will reduce the filtering effort



Simulation strategy used to define nominal filter values

- Use a simulator with good stability
- Model function with ideal switches: as switching speed gets relevant at much higher frequencies than the frequencies defining filter size it can be neglected in the first run
- Develop the filter starting from the switching semiconductors and directly connected components: building up and testing the simulation step by step helps to eliminate mistakes
- Add parasitic capacitances in very early stage of filter development: Semiconductor to heat sink, cable+motor capacitance, transformer capacitance
- Filter design by alternating high impedance components (chokes) and low impedance components (capacitors)
- Add some damping to reduce resonances

